patterning said conductive layer by an etching process using said second photoresist pattern layer, each of said dummy gate patterns being a reduction of a corresponding one of said dummy area patterns.

38. The method as claimed in claim 37, wherein the shape of at least one said dummy area patterns and/or dummy gate patterns is a circle.

39. The method as claimed in claim 37, wherein a plurality of said dummy area patterns and/or dummy gate patterns are arranged in at least two rows and/or two columns.

40. The method as claimed in claim 39, wherein at least one said row is shifted from another said row and/or at least one column is shifted from another said column.

41. A method for manufacturing a semiconductor device, comprising the steps of:

forming a plurality of dummy active areas on a semiconductor substrate by using a first mask; and

forming a plurality of dummy gates on said dummy active areas by using a second mask corresponding to said first mask.--

REMARKS

The specification has been amended to correct minor clerical errors. No new matter has been entered. Pursuant to 37 CFR 1.121, marked copies of the specification paragraphs showing the changes made therein accompany this amendment.

Claims 33-36 have been canceled without prejudice. Claims 37-41 have been added to better define and scope the instant invention.

Turning to the previous rejection of claims 33-36 under 35 USC § 103, the claims have been rewritten to better define the instant invention over the prior art. The present claimed invention exhibits an effect in that the additional design time for the dummy gate patterns can be

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